CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent ~~Application No. 10/158,193~~ 6,720,798, Filed: May 31, 2002, Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, inventors: Mulder et al., which is a Continuation-in-Part of Application No. 10/153,709, now U.S. Patent 6,628,224 Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; and is related to Application No. 10/158,774, now U.S. Patent 6,697,005 Filed: May 31, 2002; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al.; Application No. 10/158,595, now U.S. Patent 6,573,853 Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,773, now U.S. Patent 6,583,747 Filed: May 31, 2002, Inventor: Jan MULDER; Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES et al., all of which are incorporated by reference herein.

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BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to line drivers, and more particularly to high-speed, low-distortion line drivers.

Related Art

[0003] **FIG. 1** shows a conventional output driver cell of a line driver currently employed in (Gigabit) Ethernet products. Each cell includes two differential pairs, enabling tri-state operation. Transistors **M1a** through **M1d** are cascodes, implemented using thick-oxide transistors. Transistors **M3a** and **M3b** implement the tail current sources of the two differential pairs, each